REMARKS

This amendment is submitted in response to the Final Office Action dated June 29, 2006. Reconsideration and allowance of the claims is requested. In this Final Office Action, claims 1-5, 7-11, 13-20 are rejected under 35 U.S.C. 103 as unpatentable over Suzuki (US 5,694,613) considered with Bartkowiak (US 5,771,362). Claims 6 and 12 are rejected under 35 U.S.C. 103 as unpatentable over Suzuki considered with Bartkowiak and in further view of Edwards (US 5,534,796). These rejections are respectfully traversed.

By this response, in the interest of expediting the prosecution of this application, Applicant has combined claims 1, 3, and 4 into amended independent claim 1 and combined claims 7, 9, and 10 into amended independent claim 7. These claims obviously do not present any new issue and clearly are allowable over the art cited for the reasons set forth below. Independent claim 13 is also clearly allowable over the art of record.

The claims are directed to more efficient pipelined execution of instructions by providing input registers at the input end of the different functional units of the adaptable computing engine. The input registers enable a data value to be used if that value is ready at a time just before the execution stage of an instruction, rather than requiring the needed data to be a value available at a fetch stage of the instruction. These features were added to claims 1 and 7 in the previous amendment, and are not shown in the references cited. The Examiner concedes that Suzuki does not teach these features. The Examiner alleges that it would be obvious to combine Bartkowiak's teaching of input registers 32 with Suzuki's teachings at column 7. However, while Bartkowiak teaches single cycle calculations, Suzuki's teachings at column 7 are clearly based on multiple cycle calculations. Moreover, Suzuki's only alternative approach, which is arguably a single cycle configuration (column 5, line 53 through column 6, line 5), teaches that the stored data can be retained only during the timeslot for which the information is available or applied. This restriction forecloses the possibility of incorporating Bartkowiak's teachings into Suzuki. Therefore, contrary to the Examiner's position, the two references cannot be combined.

To further clarify the distinctions between the present invention and the references cited, Applicant has incorporated limitations to claims 1 and 7 taken from dependant claims 3 and 4 (into claim 1) and claims 9 and 10 (into claim 7). These limitations describe the preferred embodiment of the invention, described at beginning at the top of page 15 of the present application. In addition to registers being located at the inputs to many of the functional units in the adaptable computing engine, the preferred embodiment allows control of pairs of input pipeline registers using a 7-bit control word to allow cascading of the hardware for 72-bit operations. In these embodiments, the most significant bit of a multi-bit field determines whether one or both of the input pipeline registers in a pair are loaded, and the remaining six bits denote the data path line from where the loaded data is obtained (see tables I-IV of the present application). The use of this feature in combination with being able to use a data value if that value is ready at a time just before the execution stage of an instruction provides a scope and speed of operation that is simply is not taught or suggested in the prior art.

As against the features of claims 3, 4, 9 and 10, the Examiner cites Suzuki. However, the detailed description of Suzuki (figure 13) indicates that the pairs of registers are not coupled as claimed or utilized as claimed. The detailed description at column 7 clearly teaches that the registers 32 and 34 are paired, and registers 102 and 106 are paired, each pair holding a different instruction for a different period of time, with the instruction being moved from one pair to another pair when a clock signal is applied to the control gates 114 and 116. Clearly this is not the operation which is disclosed and now recited in the amended independent claims.

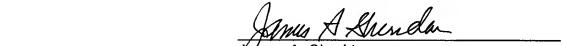
Finally, dependent claims 6 and 12 which depend on claims 1 and 7 respectfully, recite the use of seven control bits to load the paired input registers claimed above. The Examiner cites the Edwards reference against this feature, but it is clear that the Edwards teachings cannot be combined with Suzuki. Suzuki's control gates 114 and 116 which control the loading of the pairs of registers 32, 34 and 102, 106 are clearly taught to be bi-stable. Thus, they are incapable of adopting the multiple states that would be incorporated into the system of Suzuki from the teaching of Edwards with the Examiner suggested combination.

The Examiner rejects claim 13 and its dependent claims over the same combination of Suzuki and Bartkowiak. However, a careful review of both these references shows that neither reference teaches the limitation in the third paragraph of claim 13, that is, the input register being configured to store a value received from the bus at a beginning or end of a first clock cycle. As pointed out at the paragraph bridging the bottom of page 18 and the top of page 19 of the present application, the invention allows a value to be moved from a data path to an input pipeline register at the beginning or end of a clock cycle. Therefore, the value is available before the execution stage of exemplary instruction 162 commences, allowing that instruction to execute without delay and the next instruction 164 to execute in turn. The Examiner does not cite any evidence against this limitation.

Claims 2, 8, and 14, all recite that the present approach allows the inclusion of circuitry for selectively providing a constant value to the input register. As against this limitation, the Examiner again cites Suzuki, lines 19-50. However, these cited teachings only describe loading data and instructions into the pairs of registers, e.g. 32, 34, as described above. There is absolutely no teaching of a capability of loading a constant value into the registers, as described and claimed herein.

By this Preliminary Amendment, claims 6 and 12 are further amended to claim features that the Examiner contends are not clearly recited in the amendment dated October 27, 2006. New claim 22 adds a further significant feature that the teaching of the pair of pipeline registers may be selectively controlled by a bit in the control word. In view of all these distinctions, reconsideration and allowance of the claims is requested.

Respectfully submitted,



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